DAVICOM Semiconductor, Inc.

DM9119INX

Gigabit Ethernet Transceiver

DATA SHEET

Version: DM9119INX-11-MCO-DS-P01

June 1, 2020

Content

1 General Description

The DM9119INX is a single-chip Gigabit Ethernet Transceiver, which is compliant with IEEE 802.3 Media Access Controller, and IEEE 802.3u 1000BASE-T/100BASE-TX/10BASE-T. It also supports IEEE 802.3az, Energy Efficient Ethernet (EEE). The advanced on-chip mixed signal processing such as equalization, crosstalk cancellation, clock recovery, error correction, crossover detection/correction, polarity correction, provide robust transmission and reception over the standard Unshielded Twisted Pair (UTP) CAT6/CAT5e/CAT5/ CAT3(10Mbps only) cable.

The DM9119INX supports the Reduced Gigabit Media Independent Interface (RGMII) to the MAC controller.

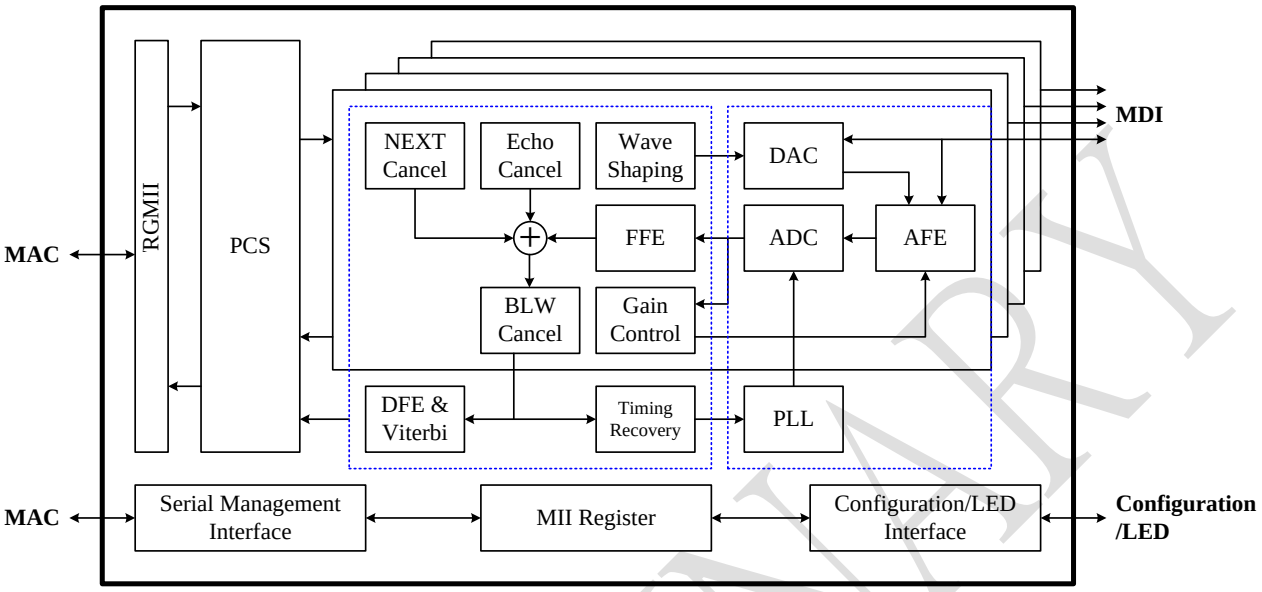
2 Features

- **Integrated 10/100/1000 Mbps Transceiver**
- **Compliant with IEEE 802.3, IEEE 802.3u, and IEEE 802.3ab**
- **Support IEEE P802.3az Energy Efficient Ethernet**
- **Auto-Negotiation with auto MDI/MDI Crossover correction**
- **Support Parallel Detection**
- **Auto Polarity Correction**
- **Advanced DSP for baseline wander correction, equalization, echo, and crosstalk Cancellation**
- **Support 3 programmable LAN status LEDs**
- **Support Power Down Mode**
- **Support RGMII MAC interface**
- **3.3V/1.25V power supply and multi-voltage I/O 3.3V to 2.5V**
- **Industrial temperature range -40 ℃ ~ + 85 ℃**
- **48-pin QFN package**

3 Application

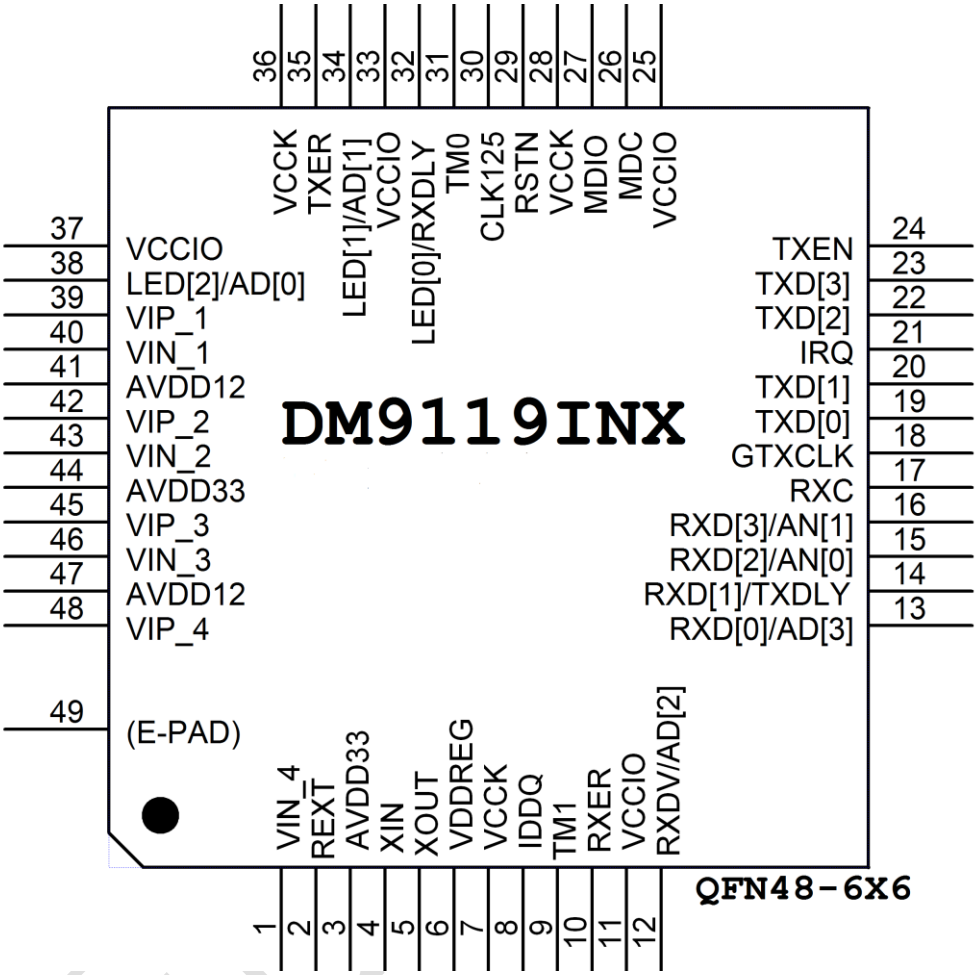
- **Network Interface Adapter**
- **Surveillance Camera**
- **Embedded System**
- **Ethernet Hub**
- **Ethernet Switch**

4 Block Diagram



5 Pin Configuration

5.1 QFN 48-Pin Package



6 Pin List Table

No.	Pin Name	No.	Pin Name
1	VIN_4	25	VCCIO
2	REXT	26	MDC
3	AVDD33	27	MDIO
4	XIN	28	VCCK
5	XOUT	29	RSTN
6	VDDREG	30	CLK125
7	VCCK	31	TM0
8	IDDQ	32	LED[0]/RXDLY
9	TM1	33	VCCIO
10	RXER	34	LED[1]/AD[1]
11	VCCIO	35	TXER
12	RXDV/AD[2]	36	VCCK
13	RXD[0]/AD[3]	37	VCCIO
14	RXD[1]/TXDLY	38	LED[2]/AD[0]
15	RXD[2]/AN[0]	39	VIP_1
16	RXD[3]/AN[1]	40	VIN_1
17	RXC	41	AVDD12
18	GTXCLK	42	VIP_2
19	TXD[0]	43	VIN_2
20	TXD[1]	44	AVDD33
21	IRQ	45	VIP_3
22	TXD[2]	46	VIN_3
23	TXD[3]	47	AVDD12
24	TXEN	48	VIP_4

7 Pin Description

Pin Type	Definition
A	Analog
D	Digital
P	Power
IO	Bi-directional
I	Input
O	Output
OD	Open drain output
L	Internal weekly pull-low
H	Internal weekly pull-high

7.1 Ethernet Transceiver Interface

Pin Name	Pin no.	Type	Description
VIP_1, VIN_1	39,40	AIO, OD	**Media Dependent Interface [0].** In MDI mode, 1000BASE-T: BI_DA+/- pair 100BASE-TX/10BASE-T: transmit pair In MDI crossover mode, 1000BASE-T: BI_DB+/- pair 100BASE-TX/10BASE-T: receive pair.
VIP_2, VIN_2	42,43	AIO, OD	**Media Dependent Interface [1].** In MDI mode, 1000BASE-T: BI_DB+/- pair 100BASE-TX/10BASE-T: receive pair In MDI crossover mode, 1000BASE-T: BI_DA+/- pair 100BASE-TX/10BASE-T: transmit pair.
VIP_3, VIN_3	45,46	AIO, OD	**Media Dependent Interface [2].** In MDI mode, 1000BASE-T: BI_DC+/- pair 100BASE-TX/10BASE-T: Unused In MDI crossover mode, 1000BASE-T: BI_DD+/- pair 100BASE-TX/10BASE-T: Unused.
VIP_4, VIN_4	48,1	AIO, OD	**Media Dependent Interface [3].** In MDI mode, 1000BASE-T: BI_DD+/- pair 100BASE-TX/10BASE-T: Unused In MDI crossover mode, 1000BASE-T: BI_DC+/- pair 100BASE-TX/10BASE-T: Unused.

7.2 Clock Interface

Pin Name	Pin no.	Type	Description
XIN	4	AI	**Crystal Input/Oscillator Input.** It is connected to a 25MHz crystal or crystal oscillator.
XOUT	5	AO	**Crystal Output.** It is connected to a crystal. When crystal oscillator is applied, this pin should be reserved as No Connection (NC).
CLK125	30	DO	**125MHz Clock Output** This signal is always present after power on and it can be turned off by powering down DM9119 using Register 0, bit 11 power down.

7.3 RGMII Interface

Pin Name	Pin no.	Type	Description
GTXCLK	18	DI	**RGMII Transmit Clock** 1000Mbps: 125MHz 100Mbps : 25MHz 10Mbps: 2.5MHz
TX_CTL (TXEN)	24	DI	**RGMII Transmit Control.** This signal presents ***TXEN*** function on the rising-edge of **GTXCLK**, and logical derivative of ***TXEN*** and ***TXER*** on the falling-edge.
TXD[3:0]	23,22, 20,19	DI	**RGMII Transmit Data** The transmit data bit [3:0] is on the rising-edge of **GTXCLK**.
RXC	17	DO	**RGMII Receive Clock** 1000Mbps: 125MHz 100Mbps : 25MHz 10Mbps: 2.5MHz
RX_CTL (RXDV)	12	DO	**RGMII Receive Control.** This signal presents ***RXDV*** function on the rising-edge of **RXC**, and logical derivative of ***RXDV*** and ***RXER*** on the falling-edge.
RXD[3:0]	16,15, 14,13	DO	**RGMII Receive Data** The receive data bit [3:0] is on the rising-edge of **RXC**.

7.4 LED Interface

Pin Name	Pin no.	Type	Description
LED[0]	32	DO	**LAN Status LED Indicator 0.** The default function is **Link 1000**, active low.
LED[1]	34	DO	**LAN Status LED Indicator 1.** The default function is **Link 100**, active low.
LED[2]	38	DO	**LAN Status LED Indicator 2.** The default function is **Link or TX/RX access**, active low.

7.5 Serial Management Interface

Pin Name	Pin no.	Type	Description
MDC	26	DI	**Serial Clock Line**
MDIO	27	DIO,H	**Serial Data Line**
IRQ	21	DO	**Interrupt to MAC**

7.6 Control and Configuration Interface

Pin Name	Pin no.	Type	Description
RSTN	29	DI	**Global Reset Input** Active-low to reset the entire chip. 0: Reset. 1: Normal operation.
IDDQ	8	DI,L	**IDDQ Test Mode** 0: Normal operation. 1: Test mode.
TM1	9	DI,L	**Test Mode 1.** 0: Normal operation. 1: Test mode.
TM0	31	DI,L	**Test Mode 0.** 0: Normal operation. 1: Test mode.
RXD[0] /AD[3] **RXDV/AD[2]** **LED[1] /AD[1]** **LED[2] /AD[0]**	13 12 34 38	DI,L	**PHY Address.** *This pin function is power on strapping.*
LED[0]/RXDLY	32	DI,H	**RGMII RXC clock delay** 0: Disable (RXC transition when data transitions) 1: Enable (RXC transition when data stable) *This pin function is power on strapping.*
RXD[1]/TXDLY	14	DI,H	**RGMII internal transmit clock(GTXCLK) delay** 0: Disable 1: Enable *This pin function is power on strapping.*
RXD[3]/AN[1] **RXD[2]/AN[0]**	16 15	DI,H	**Auto-Negotiation Configuration** 00: Advertise 1000BASE-T full duplex only. 01: Advertise 1000BASE-T full and half duplex only. 10: Advertise all capability except 1000BASE-T half duplex. 11: Advertise all capabilities. *This pin function is power on strapping.*

7.7 Power Supply

Pin Name	Pin no.	Type	Description
VDDREG	6	AP	**Connect VDDREG to 3.3V**
AVDD33	3,44	AP	**Analog Power Input** Connect to a 3.3V power source.
AVDD12	41,47	AP	**Analog Power Input** Connect to a 1.25V power source.
VCCIO	11,25,33, 37	DP	**Digital IO Power Input.** Connect to 2.5V or 3.3V power source.
VCCK	7,28,36	DP	**Digital Core Power Input.** Connect to 1.25V power source.
REXT	2	AO	**Reference Resistance.** A 12KΩ±1% external resistor is connected between this pin and ground.
E-PAD		P	**Ground.**

8 Function Description

8.1 Media Interface

The DM9119INX supports the copper interface, consists of VIP/VIN[4:1] to operate at 1000Mbps, 100Mbps, 10Mbps speed modes over standard CAT 5 unshielded twisted pair (UTP) and CAT 3 UTP (10Mbps mode only) or higher grade cables.

8.2 MAC Interface

The RGMII follows Reduced Gigabit Media Independent (RGMII)–Version 2.0. The timing could be further configured by hardware power on strapping pins to support Reduced Gigabit Media Independent (RGMII)–Version 1.3.

Table 1 RGMII Signals

Pin Name	Description
GTXCLK	**RGMII Transmit Clock** 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
TX_CTL (TXEN)	**RGMII Transmit Control.** The TXEN is on the rising-edge of GTXCLK, and logical derivative of TXEN and TXER is on the falling-edge.
TXD[3:0]	**RGMII Transmit Data** The transmit data bit [3:0] is on the rising-edge of GTXCLK, and bit [7:4] is on the falling-edge.
RXC	**RGMII Receive Clock** 1000Mbps: 125MHz 100Mbps: 25MHz 10Mbps: 2.5MHz
RX_CTL (RXDV)	**RGMII Receive Control.** The RXDV is on the rising-edge of RXC, and logical derivative of RXDV and RXER is on the falling-edge.
RXD[3:0]	**RGMII Receive Data** The receive data bit [3:0] is on the rising-edge of RXC, and bit [7:4] is on the falling-edge.

8.3 Hardware Configuration

The DM9119INX performs the hardware configuration by power on strapping pins. The PHY address, Auto-Negotiation capability and MDI Crossover correction ability are determined by properly connecting the pins to pull-up or pull-down at power on reset phase. The capability of Auto Negotiation and MDI Crossover correction ability could be changed by overwriting registers.

8.4 Serial Management Interface

The management interface is compliant to IEEE 802.3u clauses 22, which access the internal registers through the MDC and MDIO pins. The MDC signal is the reference clock, and the MDIO is the management data input/output running synchronously to MDC. The MDIO pin requires a 1.5K to 10KΩ pull-up resistor to maintain the high-level during idle and turnaround. The preamble suppression (register 1.6 =1) is supported.

The typical MDIO Frame Format is as below. PHY address is determined in Hardware Configuration process.
Idle→Start of Frame→OP Code→PHY Address→Register Address→Turnaround→Register Data→ Idle

Table 2 Serial Management Protocol

Pin Name	Description
Start of Frame	01
OP Code	Read = 10 Write = 01
PHY Address	5-bit PHY Address
Register Address	5-bit Target Register Address
Turnaround	Read = z0 Write = 10
Register Data	16-bit Target Data

Figure 1 MDC/MDIO Read Timing

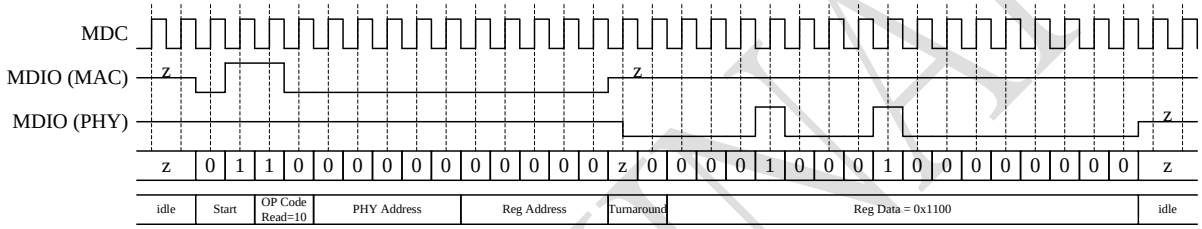
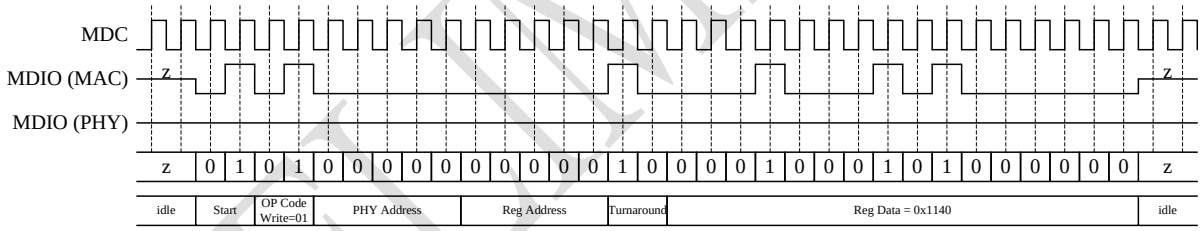


Figure 2 MDC/MDIO Write Timing



8.5 LAN Status LED Function

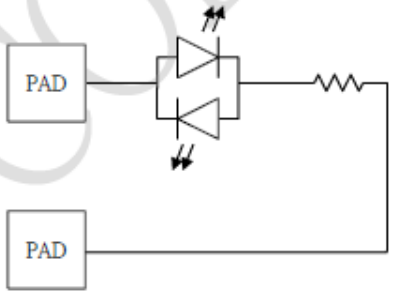
The DM9119INX supports 3 LED pins. Register 25, shown in Table 4, controls the operation mode of the LEDs.

Table 3 Operation Mode Control of LAN_LED[2:0]

Address	Register Name	Description
25.11:8	LED[2] Mode Control	0000: On- Link, Off- Not Link **0001: On- Link, Blink- Activity, Off- Not Link. (Default)** 0010: Output as interrupt. 0011: On- Activity, Off- No Activity. 0100: Blink- Activity, Off- No Activity. 0101: On- Transmit, Off- Not Transmit. 0110: On- 10/1000Mbps Link, Off- Else. 0111: On- 10Mbps Link, Off- Else. 1000: Force Off. 1001: Force On. 1011: Force Blink. Others: Reserved.
25.7:4	LED[1] Mode Control	0000: Link, Off- Not Link. 0001: On- Link, Blink- Activity, Off- Not Link. 0010: On- Link, Blink- Receive, Off- Not Link. 0011: On- Activity, Off- No Activity. 0100: Blink- Activity, Off- No Activity. 0110: On- 100/1000Mbps Link, Off- Else. **0111: On- 100Mbps Link, Off- Else. (Default)** 1000: Force Off. 1001: Force On. 1010: 10Mbps Link, Off- Else. 1011: Force Blink. Others: Reserved.
25.3:0	LED[0] Mode Control	0000: On- Link, Off- Not Link 0001: On- Link, Blink- Activity, Off- Not Link. 0010: Number of consecutive Blinks 3 Blinks – 1000Mbps 2 Blinks – 100Mbps 1 Blink – 10 Mbps 0 Blink – No Link 0011: On- Activity, Off- No Activity. 0100: Blink- Activity, Off- No Activity. 0101: On- Transmit, Off- No Transmit. 0110: On- Link, Off- Not Link **0111: On- 1000 Link, Off- Else. (Default)** 1000: Force Off. 1001: Force On. 1011: Force Blink. 1110: Dual LED Mode. Others: Reserved.

On and Off are determined by Register 24.[5:0] LED[x] Polarity Control, where x = 0 to 2.
Blink rate is configured by Register 24.15:13, LED Blink Rate Control and Register 25.15:13, LED Stretch Control.

Dual LED Connection:



In Dual LED Mode, the mixing function creates the 3rd color by driving LED[0] and LED[1] with a 20msec, opposite polarity clock. The behavior of Dual LED Mode is shown in Table 5.

Table 4 Dual LED Mode

LED[1]	LED[0]	Status
Off	Off	No Link
Off	On	1000Mbps Link – No Activity
Off	Blink	1000Mbps Link – Activity
Mix	Mix	100Mbps Link – No Activity
Blink Mix	Blink Mix	100Mbps Link – Activity
On	Off	10Mbps Link – No Activity
Blink	Off	10Mbps Link – Activity

The pulse-stretching and blink rate are also programmable by register 25.15:13 and 24.15:13. Pulse duration stretching avoids the status event is too short to be observed on the LED. The settings are applied for all LED required to blink instead of solid on.

Table 5 Pulse-Stretching and Blink Rate Control

Register	Name	Description
24.15:13	LED Blink Rate Control	000: 42msec 001: 84msec **(Default)** 010: 170msec 011: 340msec 100: 670msec Others: Reserved
25.15:13	LED Stretch Control	000: No pulse stretching 001: 42msec 010: 84msec **(Default)** 011: 170msec 100: 340msec 101: 670msec 110: 1.3sec 111: 2.7sec

8.6 Interrupt

The DM9119INX supports an interrupt signal to MAC controller. Register 18 is the Interrupt Control register, which determines what the interrupt event will generate an interrupt signal or not. Register 19 is the Interrupt Status register, which records the interrupt event and is independent of Register 18. Register 19 will keep the interrupt event until Register 19 is read (register 19 is read clear).

9 Register Description

9.1 Register Map

Address	Name
0	Basic Control Register
1	Basic Status Register
2	PHY Identifier 1
3	PHY Identifier 2
4	Auto-Negotiation Advertisement Register
5	Auto-Negotiation Link Partner Ability Register
6	Auto-Negotiation Expansion Register
7	Next Page Transmit Register
8	Link Partner Ability Next Page Register
9	1000BASE-T Control Register
10	1000BASE-T Status Register
11-14	Reserved
15	Extended Status Register
16	PHY Specific Control Register
17	PHY Specific Status Register
18	PHY Specific Interrupt Control Register
19	PHY Specific Interrupt Status Register
20	PHY Specific MDI Control and Status Register
21	PHY Specific Received Error Counter
22	PHY Specific Open/Short Test Control Register
23	PHY Specific Cable Length Status Register
24	PHY Specific LED Control Register 1
25	PHY Specific LED Control Register 2
26	PHY Specific Test Mode Control and Status Register
27	PHY Specific Configuration Register
28	PHY Specific Cable Diagnostic Register
29	PHY Specific BIST Control and Status Register
30	PHY Specific: Reserved.
31	PHY Specific: Reserved.

RW = READ and WRITE

RO = READ Only

RW/C = READ and WRITE / Clear on READ

RO/C = READ Only / Clear on READ

LH = Latched HIGH and Clear on READ to LOW

LL = Latched LOW and Clear on READ to LOW

b = Binary

h = Hexadecimal

9.2 Register Map

9.2.1 Register 0: Basic Control

Bit	Name	Description	Access	Default
0.15	Reset	0: Normal operation 1: PHY reset	RW/C	0b
0.14	Loopback	0: Normal operation 1: Enable loopback mode In loopback mode, data from TXD is looped back to RXD Link is broken when loopback mode is enabled	RW	0b
0.13	Speed Selection (LSB)	When Auto-negotiation is disabled, link speed is determined by register 0, bit 6 and bit 13 [0.6, 0.13] 0,0: 10Mbps 0,1: 100Mbps 1,0: 1000Mbps 1,1: Reserved	RW	0b
0.12	Auto-Negotiation Enable	0: Disable Auto-Negotiation 1: Enable Auto-Negotiation	RW	1b
0.11	Power Down	0: Normal operation 1: Power down	RW	0b
0.10	Isolate	0: Normal operation 1: Isolate RGMII interface	RW	0b
0.9	Restart Auto-Negotiation	0: Normal operation 1: Restart Auto-Negotiation	RW/C	0b
0.8	Duplex Mode	0: Half duplex mode 1: Full duplex mode This bit is valid in force mode only	RW	1b
0.7	Collision Test	This bit has no effect	RW	0b
0.6	Speed Selection (MSB)	Speed Selection MSB Refer to register 0 bit 13	RW	1b
0.5:0	Reserved	Reserved	RO	00h

9.2.2 Register 1: Basic Status

Bit	Name	Description	Access	Default
1.15	100BASE-T4	0: Does not support 100BASE-T4 1: Supports 100BASE-T4	RO	0b
1.14	100BASE-X Full Duplex	0: Does not support full duplex 100BASE-X 1: Supports full duplex 100BASE-X	RO	1b
1.13	100BASE-X Half Duplex	0: Does not support half duplex 100BASE-X 1: Supports half duplex 100BASE-X	RO	1b
1.12	10Mbps Full Duplex	0: Does not support full duplex 10Mbps 1: Supports full duplex 10Mbps	RO	1b
1.11	10Mbps Half Duplex	0: Does not support half duplex 10Mbps 1: Supports half duplex 10Mbps	RO	1b
1.10	100BASE-T2 Full Duplex	0: Does not support full duplex 100BASE-T2 1: Supports full duplex 100BASE-T2	RO	0b
1.9	100BASE-T2 Half Duplex	0: Does not support half duplex 100BASE-T2 1: Supports half duplex 100BASE-T2	RO	0b
1.8	Extended Status	0: No extended status information in Register 15 1: Extended status information in Register 15	RO	1b
1.7	Reserved	Reserved	RO	0b
1.6	MF Preamble Suppression	0: Does not accept management frames with preamble suppressed 1: Accepts management frames with preamble suppressed	RO	1b
1.5	Auto-Negotiation Complete	0: Auto-Negotiation process is not completed 1: Auto-Negotiation process completed	RO	0b
1.4	Remote Fault	0: No remote fault condition detected 1: Remote fault condition detected	RO, LH	0b
1.3	Auto-Negotiation Ability	0: PHY is not able to perform auto-negotiation 1: PHY is able to perform auto-negotiation	RO	1b
1.2	Link Status	0: Link is down 1: Link is up	RO, LL	0b
1.1	Jabber Detect	0: No jabber condition is detected 1: Jabber condition is detected	RO, LH	0b
1.0	Extended Capability	0: Basic register capabilities only 1: Extended register capabilities	RO	1b

9.2.3 Register 2: PHY Identifier 1

Bit	Name	Description	Access	Default
2.15:0	PHY Identifier 1	PHY Identifier 1	RO	006Eh

9.2.4 Register 3: PHY Identifier 2

Bit	Name	Description	Access	Default
3.15:0	PHY Identifier 2	PHY Identifier 2 The OUI is 0x001B8C Model Number is 6'b100001 Revision Number is 4'b0010	RO	3212h

9.2.5 Register 4: Auto-Negotiation Advertisement

Bit	Name	Description	Access	Default
4.15	Next Page	0: Next pages are not supported 1: Next pages are supported	RW	0b
4.14	Reserved	Reserved	RO	0b
4.13	Remote fault	0: Remote Fault bit is NOT SET 1: Remote Fault bit is SET	RW	0b
4.12	Reserved	Reserved	RO	0b
4.11	Asymmetric Pause	0: No support of asymmetric pause 1: Advertise support of asymmetric pause	RW	0b
4.10	Pause	0: No support of pause capability 1: Advertise support of pause capability	RW	0b
4.9	100Base-T4	0: Not capable of 100BASE-T4	RW	0b
4.8	100Base-TX Full Duplex	0: No support of 100BASE-TX full duplex 1: Advertise support of 100BASE-TX full duplex	RW	H/W Config
4.7	100Base-TX Half Duplex	0: No support of 100BASE-TX half duplex 1: Advertise support of 100BASE-TX half duplex	RW	H/W Config
4.6	10Base-TX Full Duplex	0: No support of 10BASE-T full duplex 1: Advertise support of 10BASE-T full duplex	RW	H/W Config
4.5	10Base-TX Half Duplex	0: No support of 10BASE-T half duplex 1: Advertise support of 10BASE-T half duplex	RW	H/W Config
4.4:0	Selector Field	Bit [4:0] = 5'b00001 to indicate supporting IEEE 802.3 CSMA/CD	RO	01h

9.2.6 Register 5: Auto-Negotiation Link Partner Ability

Bit	Name	Description	Access	Default
5.15	Next Page	Next Page Indication Received Code Word Bit 15	RO	0b
5.14	Acknowledge	Acknowledge Received Code Word Bit 14	RO	0b
5.13	Remote Fault	Remote Fault Indicated by Link Partner Received Code Word Bit 13	RO	0b
5.12:5	Technology Ability Field	Received Code Word Bit 12:5	RO	00h
5.4:0	Select Field	Received Code Word Bit 4:0	RO	00h

9.2.7 Register 6: Auto-Negotiation Expansion

Bit	Name	Description	Access	Default
6.15:5	Reserved	Reserved	RO	000h
6.4	Parallel Detection Fault	0: A Fault has not been detected in Parallel Detection 1: A Fault has been detected in Parallel Detection	RO, LH	0b
6.3	Link Partner Next Page Ability	0: Link Partner does not support Next Page 1: Link Partner supports Next Page	RO	0b
6.2	Next Page Capability	0: Local device does not support Next Page 1: Local device supports Next Page	RO	0b
6.1	Page Received	0: A new Page has not been received 1: A new Page has been received	RO, LH	0b
6.0	Link Partner Auto-Negotiation Ability	0: Link Partner does not support Auto-Negotiation 1: Link Partner supports Auto-Negotiation	RO	0b

9.2.8 Register 7: Next Page Transmit

Bit	Name	Description	Access	Default
7.15	Next Page	Next Page Indication Transmit Code Word Bit 15	RW	0b
7.14	Reserved	Transmit Code Word Bit 14	RO	0b
7.13	Message page	Message Page 0: Unformatted Page 1: Message Page Transmit Code Word Bit 13	RW	1b
7.12	Acknowledge 2	Acknowledge 2 0: Local device has no ability to comply with the message received 1: Local device has the ability to comply with the message received Transmit Code Word Bit 12	RW	0b
7.11	Toggle	Toggle bit Transmit Code Word Bit 11	RO	0b
7.10:0	Message / Unformatted Code Field	Content of message / unformatted Page Transmit Code Word Bit 10:0	RW	001h

9.2.9 Register 8: Link Partner Ability Next Page

Bit	Name	Description	Access	Default
8.15	Next Page	Received Code Word Bit 15	RO	0b
8.14	Acknowledge	Received Code Word Bit 14	RO	0b
8.13	Message page	Received Code Word Bit 13	RO	0b
8.12	Acknowledge 2	Received Code Word Bit 12	RO	0b
8.11	Toggle	Received Code Word Bit 11	RO	0b
8.10:0	Message/Unformatted Code Field	Received Code Word Bit 10:0	RO	000h

9.2.10 Register 9: 1000BASE-T Control

Bit	Name	Description	Access	Default
9.15:13	Test Mode	Test Mode Select 000: Normal Operation 001: Test Mode 1 – Transmit waveform test 010: Test Mode 2 – Master transmit jitter test 011: Test Mode 3 – Slave transmit jitter test 100: Test Mode 4 – Transmitter distortion test Others: Reserved	RW	000b
9.12	Manual Master/Slave Enable	Enable Manual Master / Slave configuration 0: Automatic Master/Slave configuration 1: Manual Master/Slave configuration	RW	0b
9.11	Manual Master/ Slave Configuration	Advertise Master / Slave Configuration value 0: Manual configure as slave (9.12 =1) 1: Manual configure as master (9.12 =1)	RW	0b
9.10	Port Type	Advertise Device Type Preference 0: Single-port device, slave preferred (9.12=0) 1: Multi-port device, master preferred (9.12=0)	RW	0b
9.9	1000Base-T Full Duplex	0: Advertise PHY is not 1000Base-T full duplex capable 1: Advertise PHY is 1000Base-T full duplex capable	RW	1b
9.8	1000Base-T Half Duplex	0: Advertise PHY is not 1000Base-T half duplex capable 1: Advertise PHY is 1000Base-T half duplex capable	RW	H/W Config
9.7:0	Reserved	Reserved	RO	00h

9.2.11 Register 10: 1000BASE-T Status

Bit	Name	Description	Access	Default
10.15	Master/Slave Configure Fault	0: No master/Slave configuration fault detected 1: Master/Slave configuration fault detected	RO, LH	0b
10.14	Master/Slave Resolution	0: Local PHY configuration resolved to Slave 1: Local PHY configuration resolved to Master	RO	0b
10.13	Local Receiver Status	0: Local receiver is not OK 1: Local receiver OK	RO	0b
10.12	Remote Receiver Status	0: Remote receiver is not OK 1: Remote receiver OK	RO	0b
10.11	Link Partner 1000BASE-T Full-Duplex	0: Link partner is not capable of 1000Base-T full duplex 1: Link partner is capable of 1000Base-T full duplex This register will be updated when completed Auto-Negotiation	RO	0b
10.10	Link Partner 1000BASE-T Half-Duplex	0: Link partner is not capable of 1000Base-T half duplex 1: Link partner is capable of 1000Base-T half duplex This register will be updated when completed Auto-Negotiation	RO	0b
10.9:8	Reserved	Reserved	RO	00b
10.7:0	Idle Error Count	Error count when receiving wrong IDLE from Link partner in Gigabit mode The counter will stop at 255 if the error more than 255	RO/C	00h

9.2.12 Register 15: Extended Status

Bit	Name	Description	Access	Default
15.15	1000BASE-X Full Duplex	0: Does not support 1000BASE-X full duplex 1: Supports 1000BASE-X full duplex	RO	0b
15.14	1000BASE-X Half Duplex	0: Does not support 1000BBASE-X half duplex 1: Supports 1000BASE-X half duplex	RO	0b
15.13	1000BASE-T Full Duplex	0: Does not support 1000BASE-T full duplex 1: Supports 1000BASE-T full duplex	RO	1b
15.12	1000BASE-T Half Duplex	0: Does not support 1000BASE-T half duplex 1: Supports 1000BASE-T half duplex	RO	1b
15.11:0	Reserved	Reserved	RO	000h

9.2.13 Register 16: PHY Specific Control

Bit	Name	Description	Access	Default
16.15:14	Reserved	Reserved	RO	00b
16.13	Reserved	Reserved	RO	0b
16.12	1000Mbps Force Master/Slave	0: Force 1000Mbps mode in Slave 1: Force 1000Mbps mode in Master	RW	0b
16.11	1000Mbps Force Mode	0: Normal mode 1: 1000Mbps Force mode without Auto-negotiation	RW	0b
16.10	Direct Mode	0: Normal operation	RW	0b

Bit	Name	Description	Access	Default
		1: Bypass TX/RX FIFO This function only used in 10/100Mbps		
16.9	Auto Speed Down Mode	0: Disable 1: Enable	RW	0b
16.8	Statistic Counters Enable	0: Disable Register 21 Receive error counter 1: Enable Register 21 Receive error counter	RW	0b
16.7:6	Reserved	Reserved	RO	00b
16.5	RXC Output in Power Down Mode	0: Enable RXC in power down mode 1: Disable RXC in power down mode The RXC clock rate is 2.5MHz in power down mode	RW	0b
16.4	Force 10BASE-T Signal Polarity	0: Force normal received signal polarity 1: Force inverse received signal polarity	RW	0b
16.3	Force 10Mbps Mode Polarity Enable	0: Auto 10BASE-T received signal polarity 1: Manual 10BASE-T received signal polarity	RW	0b
16.2:1	Sleep Timer Select	The bits select the timer for power down in sleep mode 00: 4 sec 01: 5 sec 10: 6 sec 11: 7 sec	RW	00b
16.0	Digital Core Test Mode	0: Normal operation 1: Test mode for digital code simulation Always set to 0 in normal application	RW	0b

9.2.14 Register 17: PHY Specific Status

Bit	Name	Description	Access	Default
17.15:14	Link Speed Status	00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved	RO	00b
17.13	Duplex Status	0: Half duplex 1: Full duplex	RO	0b
17.12	Reserved	Reserved	RO	00b
17.11	Speed and Duplex Resolved Status	0: Not resolved 1: Resolved	RO	0b
17.10	Link Status	0: Link down 1: Link up	RO	0b
17.9:7	Reserved	Reserved	RO	000b
17.6	MDI Crossover Status	0: No MDI Crossover detected 1: MDI Crossover detected This Bit is valid in 10/100 Mbps mode	RO	0b
17.5:2	Reserved	Reserved	RO	0h
17.1	10BASE-T Polarity Status	0: Normal signal polarity 1: Inverse signal polarity	RO	0b
17.0	Reserved	Reserved	RO	0b

9.2.15 Register 18: PHY Specific Interrupt Control

Bit	Name	Description	Access	Default
18.15	Auto-Negotiation Fail	0: Disable Auto-Negotiation error interrupt 1: Enable Auto-Negotiation error interrupt	RW	0b
18.14	Link Speed Change	0: Disable link speed change interrupt 1: Enable link speed change interrupt	RW	0b
18.13	Duplex Change	0: Disable duplex change interrupt 1: Enable duplex change interrupt	RW	0b
18.12	Page Received	0: Disable page received interrupt 1: Enable page received interrupt	RW	0b
18.11	Auto-Negotiation Complete	0: Disable Auto-Negotiation complete interrupt 1: Enable Auto-Negotiation complete interrupt	RW	0b
18.10	Link Status Change	0: Disable link status change interrupt 1: Enable link status change interrupt	RW	0b
18.9:8	Reserved	Reserved	RO	00b
18.7	Wake on LAN packet received	0 : Disable WOL packet received interrupt 1: Enable WOL packet received interrupt	RW	0b
18.6	MDI Crossover Change	0: Disable MDI Crossover change interrupt 1: Enable MDI Crossover change interrupt	RW	0b
18.5	Reserved	Reserved	RO	0b
18.4	Power Mode Change	0: Disable power mode change interrupt 1: Enable power mode change interrupt	RW	0b
18.3	Cable Diagnostic Complete	0: Disable cable diagnostic complete interrupt 1: Enable cable diagnostic complete interrupt	RW	0b
18.2	Open/Short Diagnostic Done	0: Disable Open/Short diagnostic done interrupt 1: Enable Open/Short diagnostic done interrupt	RW	0b
18.1	Polarity Change	0: Disable polarity change interrupt 1: Enable polarity change interrupt	RW	0b
18.0	Reserved	Reserved	RO	0b

9.2.16 Register 19: PHY Specific Interrupt Status

Bit	Name	Description	Access	Default
19.15	Auto-Negotiation Fail	Auto-Negotiation fail interrupt status	RO/C, LH	0b
19.14	Link Speed Change	Link speed change interrupt status	RO/C, LH	0b
19.13	Duplex Change	Duplex change interrupt status	RO/C, LH	0b
19.12	Page Received	Page received interrupt status	RO/C, LH	0b
19.11	Auto-Negotiation Complete	Auto-Negotiation complete interrupt status	RO/C, LH	0b
19.10	Link Status Change	Link status change interrupt status	RO/C, LH	0b
19.9:8	Reserved	Reserved	RO	00b
19.7	Wake on LAN packet received	Wake on LAN packet received interrupt status	RO/C,LH	0b
19.6	MDI Crossover Change	MDI Crossover change MDI interrupt status	RO/C,LH	0b
19.5	Reserved	Reserved	RO	0b
19.4	Power Mode Change	Power mode change interrupt status	RO/C, LH	0b

Bit	Name	Description	Access	Default
19.3	Cable Diagnostic Complete	Cable diagnostic complete interrupt status	RO/C, LH	0b
19.2	Open/Short Diagnostic Done	Open/Short diagnostic done interrupt status	RO/C, LH	0b
19.1	Polarity Change	Polarity change interrupt status	RO/C, LH	0b
19.0	Reserved	Reserved	RO	0b

9.2.17 Register 20: PHY Specific MDI Control and Status

Bit	Name	Description	Access	Default
20.15	Channel D Signal Polarity	0: Normal signal polarity 1: Inverse signal polarity	RO	0b
20.14	Channel C Signal Polarity	0: Normal signal polarity 1: Inverse signal polarity	RO	0b
20.13	Channel B Signal Polarity	0: Normal signal polarity 1: Inverse signal polarity	RO	0b
20.12	Channel A Signal Polarity	0: Normal signal polarity 1: Inverse signal polarity	RO	0b
20.11:8	Reserved	Reserved	RO	0h
20.7	MDI/MDI Crossover of Channel A, B	0: Channel A, B in MDI mode 1: Channel B, A in MDI Crossover mode	RO	0b
20.6	MDI/MDI Crossover of Channel C, D	0: Channel C, D in MDI mode 1: Channel D, C in MDI Crossover mode	RO	0b
20.5	Force MDI / MDI Crossover Enable	0: Normal operation 1: Manual set MDI/MDI Crossover	RW	H/W Config
20.4	Force MDI / MDI Crossover of Channel A, B and C, D	0: Force MDI on channel A, B and C, D 1: Force MDI Crossover on channel B, A and D, C	RW	0b
20.3:1	Reserved	Reserved	RO	0h
20.0	Cable Diagnostic Done	0: Cable diagnostic is on going 1: Cable diagnostic is finished	RO	0b

9.2.18 Register 21: PHY Specific Received Error Counter

Bit	Name	Description	Access	Default
21.15:0	Receiver Data Error Counter	Count the event of when RX_ER is asserted when RX_DV is high RX_ER is caused by link partner sending TX_ER The counter will stop on 65535 (ffffh) if error more than 65535	RO/C	0000h

9.2.19 Register 22: PHY Specific Open/Short Test Control Register

Bit	Name	Description	Access	Default
22.15:2	Reserved	Reserved	RO	0000h
22.1:0	Open/Short Channel Select	00: Select Channel A 01: Select Channel B 10: Select Channel C 11: Select Channel D	RW	00b

9.2.20 Register 23: PHY Specific Link Cable Length

Bit	Name	Description	Access	Default
23.15:12	Channel D Cable Length	Estimated CAT-5 length	RW	0h
23.11:8	Channel C Cable Length	Estimated CAT-5 length	RW	0h
23.7:4	Channel B Cable Length	Estimated CAT-5 length	RW	0h
23.3:0	Channel A Cable Length	Estimated CAT-5 length 0: 0-35m 8: 110m 1: 40m 9: 120m 2: 50m 10: 130m 3: 60m 11: 140m 4: 70m 12: 150m 5: 80m 13: 160m 6: 90m 14: >170m 7: 100m 15: Reserved For reference use only	RW	0h

9.2.21 Register 24: PHY Specific LED Control Register 1

Bit	Name	Description	Access	Default
24.15:13	LED Blink Rate Control	000: 42msec 001: 84msec 010: 170msec 011: 340msec 100: 670msec Others: Reserved	RW	001b
24.12:8	FLP Gap Control	The FLP gap is [24.12:8] x 1msec	RW	0Dh
24.7:6	Reserved	Reserved	RO	00b
24.5:4	LED[2] Polarity Control	00: On- LED drive low, Off- LED drive high 01: On- LED drive high, Off- LED drive low 10: On- LED drive low, Off- LED tri-state 11: On- LED drive high, Off- LED tri-state	RW	00b
24.3:2	LED[1] Polarity Control	00: On- LED drive low, Off- LED drive high 01: On- LED drive high, Off- LED drive low 10: On- LED drive low, Off- LED tri-state 11: On- LED drive high, Off- LED tri-state	RW	00b
24.1:0	LED[0] Polarity Control	00: On- LED drive low, Off- LED drive high 01: On- LED drive high, Off- LED drive low 10: On- LED drive low, Off- LED tri-state 11: On- LED drive high, Off- LED tri-state	RW	00b

9.2.22 Register 25: PHY Specific LED Control Register 2

Bit	Name	Description	Access	Default
25.15:13	LED Stretch Control	000: No pulse stretching 001: 42msec 010: 84msec 011: 170msec 100: 340msec 101: 670msec 110: 1.3sec 111: 2.7sec	RW	010b
25.12	Reserved	Reserved	RO	0b
25.11:8	LED[2] Mode Control	0000: On- Link, Off- Not Link 0001: On- Link, Blink- Activity, Off- Not Link 0010: Output as interrupt 0011: On- Activity, Off- No Activity 0100: Blink- Activity, Off- No Activity 0101: On- Transmit, Off- Not Transmit 0110: On- 10/1000Mbps Link, Off- Else 0111: On- 10Mbps Link, Off- Else 1000: Force Off 1001: Force On 1011: Force Blink Others: Reserved	RW	1h
25.7:4	LED[1] Mode Control	0001: On- Link, Blink- Activity, Off- Not Link 0010: On- Link, Blink- Receive, Off- Not Link 0011: On- Activity, Off- No Activity 0100: Blink- Activity, Off- No Activity 0110: On- 100/1000Mbps Link, Off- Else 0111: On- 100Mbps Link, Off- Else 1000: Force Off 1001: Force On 1011: Force Blink Others: Reserved	RW	7h
25.3:0	LED[0] Mode Control	0000: On- Link, Off- Not Link 0001: On- Link, Blink- Activity, Off- Not Link 0010: 3 Blinks – 1000Mbps 2 Blinks – 100Mbps 1 Blink – 10 Mbps 0 Blink – No Link 0011: On- Activity, Off- No Activity 0100: Blink- Activity, Off- No Activity 0101: On- Transmit, Off- No Transmit 0110: On- Link, Off- Not Link 0111: On- 1000 Link, Off- Else 1000: Force Off 1001: Force On 1011: Force Blink 1110: Dual LED Mode Others: Reserved	RW	7h

9.2.23 Register 26: PHY Specific Test Mode Control Register

Bit	Name	Description	Access	Default
26.15:13	Reserved	Reserved	RO	000b
26.12:11	Sleep Mode Enable	0X: Normal operation 10: Sleep and wake up on squelch 11: Sleep and wake up on squelch and periodically	RW	00b
26.10:5	Reserved	Reserved	RO	00h
26.4	Remote Loopback Enable	0: Normal operation 1: Enable remote loopback Speed is selected by 0.6 and 0.13	RW	0b
26.3:0	Reserved	Reserved	RO	0000b

9.2.24 Register 27: PHY Specific Configuration

Bit	Name	Description	Access	Default
27.15:10	Reserved	Reserved	RW	00h
27.9	Interrupt Polarity	0: interrupt active high 1: interrupt active low	RW	0b
27.8:0	Reserved	Reserved	RO	00h

9.2.25 Register 28: PHY Specific Cable Diagnostic Register

Bit	Name	Description	Access	Default
28.15	Cable Diagnostic Enable	0: Normal operation 1: Enable cable diagnostic	RW/C	0b
28.14:13	Cable Diagnostic Result	01: Short 10: Open 00: Terminate 11: Reserved	RO	00b
28.12:8	Cable Reflection Counter	Cable Reflection Counter	RO	00h
28.7:0	Cable Open/Short Distance	Cable Open/Short Distance	RO	00h

9.2.26 Register 29: PHY Specific BIST Control and Status Register

Bit	Name	Description	Access	Default
29.15:0	Reserved	Reserved	RO	0000h

9.2.27 Register 30: PHY Specific Internal Register Map Address Port

Bit	Name	Description	Access	Default
30.15	Write Command Indicator	Write one to execute a write access associated with the address 30.7:0	RW/C	0b
30.14	Read Command Indicator	Write one to execute a read access associated with the address 30.7:0	RW/C	0b
30.13:8	Reserved	Reserved	RO	00h
30.7:0	Address Pointer for Internal Register	Address pointer for internal register map	RW	00h

9.2.28 Register 31: PHY Specific Internal Register Map Data Port

Bit	Name	Description	Access	Default
31.15:0	Data Port	Data port for internal register access	RW	0000h

10 Electrical Characteristics

10.1 Absolute Maximum Rating

Parameter	Symbol	Condition	Min	Max	Unit
Analog power supply	AVDD33		-0.4	3.96	V
Analog power supply	AVDD12		-0.4	1.6	V
Digital core power supply	VCCK		-0.4	1.6	V
Digital I/O power supply	VCCIO		-0.4	3.96	V
Digital I/O input voltage	$V_{I(D)}$		-0.4	VCCIO+0.4	V
Storage temperature	$T_{STORAGE}$		-65	150	^oC

10.2 Recommended Operation Condition

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Analog power supply	AVDD33		2.97	3.30	3.63	V
Analog power supply	AVDD12			1.25		V
Digital core power supply	VCCK			1.25		V
Digital I/O power supply	VCCIO			3.30		V
Digital I/O power supply	VCCIO			2.50		V
Ambient operation temperature	T_A		-40		+85	^oC
Junction temperature	T_J				125	^oC
Package Surface Temperature*	T_C			50		^oC

* T_A at 25 ^oC

10.3 25Mz Clock Source Requirement

Parameter	Symbol	Condition	Min	Typical	Max	Unit
25MHz Reference Clock			-30ppm	25	30ppm	MHz
25MHz Clock Duty Cycle			45	50	55	%

10.4 DC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
DC driving at $V_{OH(min)}$				8		mA
DC driving at $V_{OL(max)}$				8		mA
Output High Voltage	V_{OH}		2.4			V
Output Low Voltage	V_{OL}				0.4	V
Input High Voltage			1.5			V
Input Low Voltage					1.28	V
Weak pull high R value				70.0		kΩ
Weak pull low R value				70.0		kΩ
AC rising time				3.6		ns
AC falling time				3.8		ns
3.3V power consumption				110		mA
1.25V power consumption				270		mA

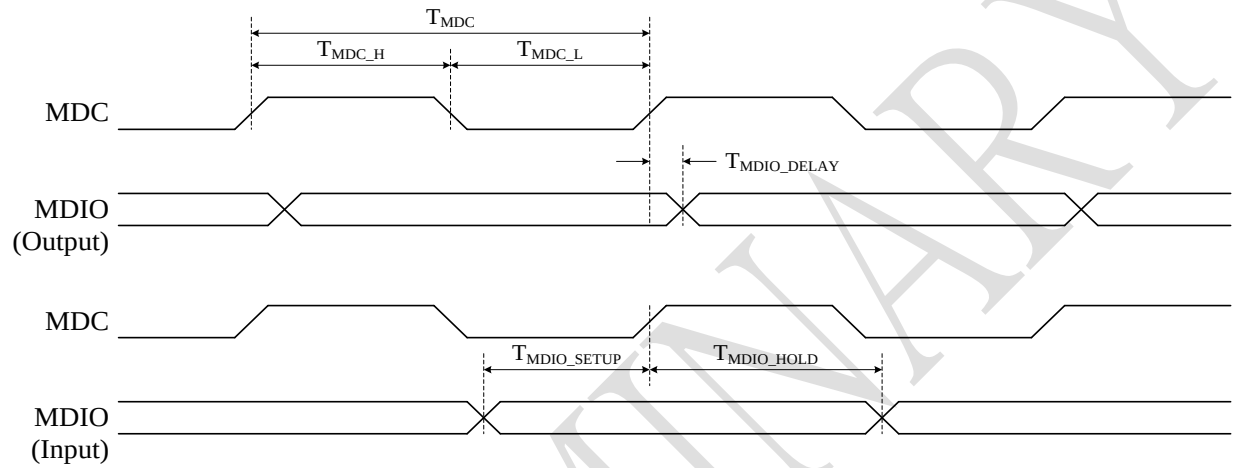
10.5 Power Sequence Requirement

Parameter	Symbol	Condition	Min	Typical	Max	Unit
3.3V Power Rise Time					300	ms

10.6 AC Characteristics

10.6.1 Serial Management Port Timing

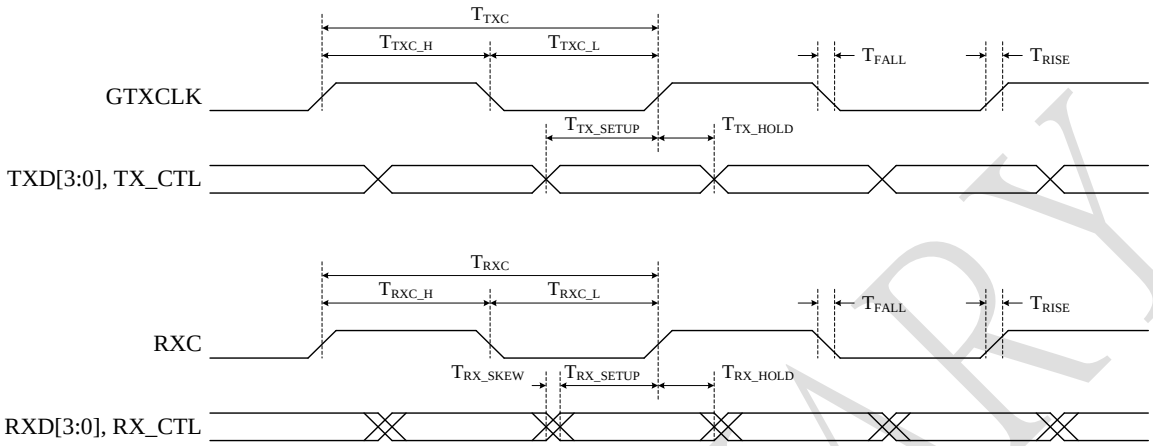
Figure 3 MDC/MDIO Timing Diagram



Parameter	Symbol	Condition	Min	Typical	Max	Unit
MDC Cycle Time	TMDC		0		10	ns
MDC Low Period	TMDC_L		5			ns
MDC High Period	TMDC_H		5			ns
MDC to MDIO Output Delay	TMDC_DELAY				5	ns
MDIO to MDC Setup Time	TMDIO_SETUP		2			ns
MDIO to MDC Hold Time	TMDIO_HOLD		2			ns

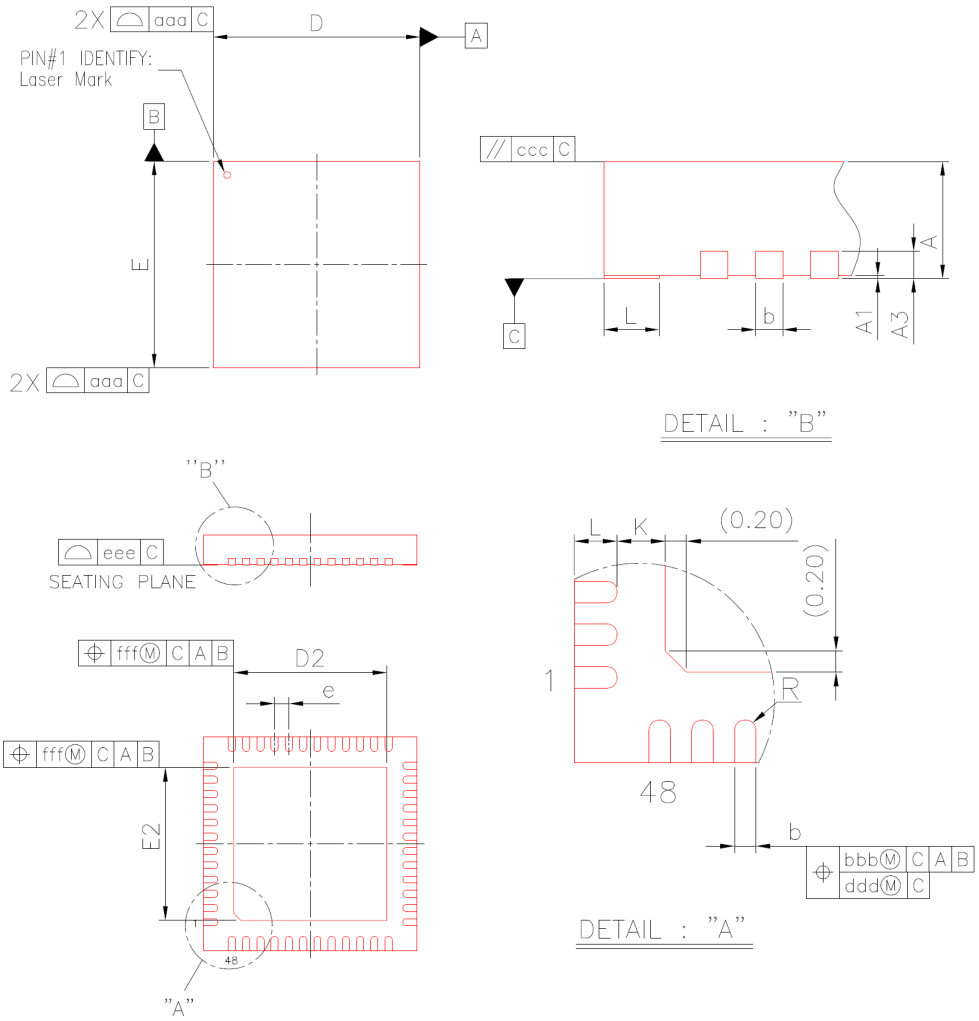
10.6.2 RGMII Interface Timing

Figure 4 RGMII Interface Timing Diagram



Parameter	Symbol	Condition	Min	Typical	Max	Unit
GTXCLK Cycle Time	TTXC	1000Mbps Link	7.2	8.0	8.8	ns
GTXCLK Low Period	TTXC_L	1000Mbps Link	3.6	4	4.4	ns
GTXCLK High Period	TTXC_H	1000Mbps Link	3.6	4	4.4	ns
TXD/TX_CTL to GTXCLK Setup Time	TTXC_SETUP	1000Mbps Link	1.2	2		ns
TXD/TX_CTL to GTXCLK Hold Time	TTXC_HOLD	1000Mbps Link	1.2	2		ns
Rise Time/Fall Time (20%-80%)	TRISE/TFALL	1000Mbps Link			0.75	ns
GTXCLK Cycle Time	TTXC	100Mbps Link	36	40	44	ns
GTXCLK Low Period	TTXC_L	100Mbps Link	16	20	24	ns
GTXCLK High Period	TTXC_H	100Mbps Link	16	20	24	ns
TXD/TX_CTL to GTXCLK Setup Time	TTXC_SETUP	100Mbps Link	1.2			ns
TXD/TX_CTL to GTXCLK Hold Time	TTXC_HOLD	100Mbps Link	1.2			ns
GTXCLK Cycle Time	TTXC	10Mbps Link	360	400	440	ns
GTXCLK Low Period	TTXC_L	10Mbps Link	160	200	240	ns
GTXCLK C High Period	TTXC_H	10Mbps Link	160	200	240	ns
TXD/TX_CTL to GTXCLK Setup Time	TTXC_SETUP	10Mbps Link	1.2			ns
TXD/TX_CTL to GTXCLK Hold Time	TTXC_HOLD	100Mbps Link	1.2			ns
RXC Cycle Time	TRXC	1000Mbps Link	7.2	8.0	8.8	ns
RXC Low Period	TRXC_L	1000Mbps Link	3.6	4	4.4	ns
RXC High Period	TRXC_H	1000Mbps Link	3.6	4	4.4	ns
RXD/RX_CTL to RXC Skew	TRX_SKEW	1000Mbps Link	-0.5		0.5	ns
RXC Cycle Time	TRXC	100Mbps Link	36	40	44	ns
RXC Low Period	TRXC_L	100Mbps Link	16	20	24	ns
RXC High Period	TRXC_H	100Mbps Link	16	20	24	ns
RXC Cycle Time	TRXC	10Mbps Link	360	400	440	ns
RXC Low Period	TRXC_L	10Mbps Link	160	200	240	ns
RXC High Period	TRXC_H	10Mbps Link	160	200	240	ns

11 Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

12 Ordering Information

Part Number	Pin Count	Package
DM9119INX	48	QFN(Pb-Free)

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Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.